

**Amendment and Response**

Applicant: Andrew Spencer

Serial No.: 10/689,244

Filed: Oct. 20, 2003

Docket No.: 10014282-1/H303.158.101

Title: SYSTEM AND METHOD FOR SETTING A CLOCK RATE OF A MEMORY CARD

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**IN THE CLAIMS**

**Amendments to the Claims**

**This listing of claims will replace all prior versions, and listings, of the claims:**

1. (Currently Amended) A memory card comprising:
  - a buffer configured to receive transactions;
  - a storage media;
  - a control circuit coupled to the buffer and the storage media; and
  - a processor system coupled to the control circuit;

a buffer management circuit coupled to the processor system and configured to provide at least one signal to the processor system that indicates when the buffer is full and when the buffer is empty;

wherein the processor system is configured to detect a rate of transactions received by the buffer by determining a number of times that the buffer is full and empty from the at least one signal over a time period, and wherein the control circuit is configured to cause a first clock signal to be provided to the buffer and the storage media at a first clock rate that varies in dependence on the detected rate of the transactions.
2. (Previously Presented) The memory card of claim 1 wherein the processor system is configured to cause the control circuit to set the first clock signal to the first clock rate associated with the rate of transactions received by the buffer.
3. (Canceled)
4. (Original) The memory card of claim 2 further comprising:
  - a master clock configured to provide a second clock signal at a second clock rate to the processor system and the control circuit;

wherein the control circuit is configured to generate the first clock signal using the second clock signal.

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5. (Original) The memory card of claim 4 wherein the first clock rate differs from the second clock rate.

6. (Original) The memory card of claim 1 further comprising:

a first interface coupled to the buffer and configured to receive the transactions from a host device and provide the transactions to the buffer; and

a second interface coupled to the buffer and the storage media.

7. (Original) The memory card of claim 1 wherein the transactions include read transactions configured to cause information to be read from the storage media.

8. (Original) The memory card of claim 1 wherein the transactions include write transactions configured to cause information to be written to the storage media.

9. (Original) The memory card of claim 1 wherein the transactions include read transactions configured to cause information to be read from the storage media and write transactions configured to cause information to be written to the storage media.

10. (Currently Amended) A system comprising:

a host device; and

a memory card configured to couple to the host device;

wherein the memory card includes a storage media, wherein the memory card is configured to count a number of transactions received by the memory card from the host device during a time period, and wherein the memory card is configured to provide a first clock signal to the storage media at a first clock rate that varies in dependence on a-the number of transactions received by the memory card from the host device during a-the time period.

11. (Currently Amended) The system of claim 10 wherein the memory card includes a processor system and a control circuit coupled to the processor system, wherein the processor

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system is configured to determine count the number of transactions received by the memory card from the host device during the time period, and wherein the processor system is configured to cause the control circuit to set the rate of the first clock signal in response to the number of transactions.

12. (Currently Amended) The system of claim 11 wherein the memory card includes a buffer and a buffer management circuit, wherein the buffer management circuit is configured to provide information to the processor system, and wherein the processor system is configured to determine count the number of transactions received by the memory card during the time period using the information.

13. (Original) The system of claim 11 wherein the memory card includes a clock configured to provide a second clock signal to the processor system and the control circuit at a second clock rate, and wherein the control circuit is configured to generate the first clock signal using the second clock signal.

14. (Original) The system of claim 10 wherein host device comprises a digital camera.

15. (Original) The system of claim 10 wherein the memory card includes a buffer and an interface coupled to the buffer, and wherein the interface is coupled to receive the transactions from the host device and provide the transactions to the buffer.

16. (Original) The system of claim 10 wherein the transactions include read transactions configured to cause information to be read from the memory card and provided to the host device.

17. (Original) The system of claim 10 wherein the transactions include write transactions configured to cause information to be written from the host device to the memory card.

18. (Original) The system of claim 10 wherein the transactions include read transactions configured to cause first information to be read from the storage media and provided to the

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host device and write transactions configured to cause second information to be written from the host device to the memory card.

19. (Currently Amended) A method comprising:

determining a first rate of transactions received by a buffer in a memory card by comparing an amount of information stored in the buffer to a threshold level;

setting a first clock signal of the memory card to a first clock rate that varies in dependence on the rate of transactions; and

providing the first clock signal to the buffer and a storage media in the memory card.

20. (Previously Presented) The method of claim 19 further comprising:

determining the first rate of transactions by monitoring the buffer of the memory card.

21-23. (Canceled)

24. (Original) The method of claim 19 further comprising:

subsequent to determining the first rate, determining a second rate of transactions received by the memory card; and

setting the first clock signal to a second clock rate associated with the rate of transactions.

25. (Original) The method of claim 19 wherein the transactions include read transactions configured to cause information to be read from the memory card.

26. (Original) The method of claim 19 wherein the transactions include write transactions configured to cause information to be written to the memory card.

27. (Original) The method of claim 19 wherein the transactions include read transactions configured to cause first information to be read from the memory card and write transactions configured to cause second information to be written to the memory card.

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28. (Currently Amended) A memory card comprising:  
a buffer configured to receive transactions;  
a storage media;  
a clock configured to generate a clock signal and provide the clock signal to the buffer  
and the storage media;

means for determining counting a rate-number of the transactions received by the  
buffer over a time period; and

means for causing the clock signal to be set at a rate associated with the rate-number  
of transactions.

29. (Original) The memory card of claim 28 further comprising:

an interface coupled to the buffer;

wherein the interface is configured to receive the transactions from a host device and  
provide the transactions to the buffer.

30. (Original) The memory card of claim 28 wherein the transactions include read  
transactions configured to cause information to be read from the storage media.

31. (Original) The memory card of claim 28 wherein the transactions include write  
transactions configured to cause information to be written to the storage media.

32. (Original) The memory card of claim 28 wherein the transactions include read  
configured to cause information to be read from the storage media and write transactions  
configured to cause information to be written to the storage media.

33. (Currently Amended) A memory card comprising:

a buffer;

an interface configured to receive transactions from a host device and provide the  
transactions to the buffer;

a storage media;

a control circuit coupled to the buffer and the storage media; and

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a processor system coupled to the control circuit;

wherein the processor system is configured to ~~detect count~~ a ~~rate number~~ of transactions received by the buffer over a time period, wherein the processor system is configured to cause the control circuit to set a first clock signal to a first clock rate that varies in dependence on the ~~rate number~~ of transactions received by the buffer, and wherein the control circuit is configured to cause the first clock signal to be provided to the buffer and the storage media.

34. (Original) The memory card of claim 33 further comprising:

a master clock configured to provide a second clock signal at a second clock rate to the processor system and the control circuit;

wherein the control circuit is configured to generate the first clock signal using the second clock signal.

35. (Original) The memory card of claim 33 wherein the transactions include read transactions configured to cause information to be read from the storage media.

36. (Original) The memory card of claim 33 wherein the transactions include write transactions configured to cause information to be written to the storage media.